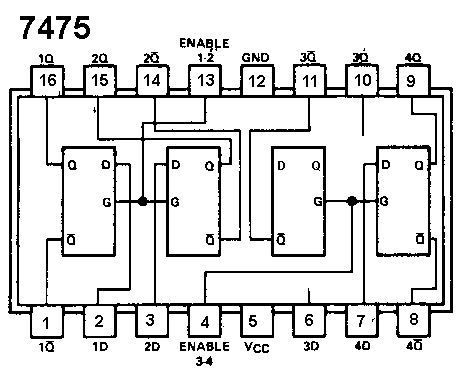
|  |  |  |
| --- | --- | --- |
| 1. | Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz. | |
|
| **[A].** | | | 10.24 kHz | |
| **[B].** | | | |  |  | | --- | --- | | 5 kHz | @ | | |
| **[C].** | | | 30.24 kHz | |
| **[D].** | | | 15 kHz | |

**Answer:** Option **B**

12 flip flops = 2^12 = 4096.  
=> 20.48\*10^6=20480000.  
  
20480000/4096 = 5000 i.e., 5 kHz.

|  |  |
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| 2. | Which statement BEST describes the operation of a negative-edge-triggered D flip-flop? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | The logic level at the *D* input is transferred to *Q* on NGT of *CLK*. | | [**B.**](javascript:%20void%200;) | The *Q* output is ALWAYS identical to the *CLK* input if the *D* input is HIGH. | | [**C.**](javascript:%20void%200;) | The *Q* output is ALWAYS identical to the *D* input when *CLK* = PGT. | | [**D.**](javascript:%20void%200;) | The *Q* output is ALWAYS identical to the *D* input. | |

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| 3. | Propagation delay time, tPLH, is measured from the \_\_\_\_\_\_\_\_. |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | triggering edge of the clock pulse to the LOW-to-HIGH transition of the output | | [**B.**](javascript:%20void%200;) | triggering edge of the clock pulse to the HIGH-to-LOW transition of the output | | [**C.**](javascript:%20void%200;) | preset input to the LOW-to-HIGH transition of the output | | [**D.**](javascript:%20void%200;) | clear input to the HIGH-to-LOW transition of the output |   **Answer:** Option **A** |
| |  |  | | --- | --- | | 4. | How is a *J-K* flip-flop made to toggle? | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | *J* = 0, *K* = 0 | | [**B.**](javascript:%20void%200;) | *J* = 1, *K* = 0 | | [**C.**](javascript:%20void%200;) | *J* = 0, *K* = 1 | | [**D.**](javascript:%20void%200;) | *J* = 1, *K* = 1 |   **Answer:** Option **D** | | |
|  | |
| 5. | How many flip-flops are in the 7475 IC? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | 1 | | [**B.**](javascript:%20void%200;) | 2 | | [**C.**](javascript:%20void%200;) | 4 | | [**D.**](javascript:%20void%200;) | 8 | |



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|
| 6. | How many flip-flops are required to produce a divide-by-128 device? |
| |  |  | | --- | --- | | **[A].** | 1 | | **[B].** | 4 | | **[C].** | 6 | | **[D].** | |  |  | | --- | --- | | 7 | @ | |   **Answer:** Option **D** |

2^7 =128  
  
=> 7 flip flops are required.

7. A J-K flip-flop is in a "no change" condition when \_\_\_\_\_\_\_\_.

|  |  |
| --- | --- |
| [**A.**](javascript:%20void%200;) | J = 1, K = 1 |
| [**B.**](javascript:%20void%200;) | J = 1, K = 0 |
| [**C.**](javascript:%20void%200;) | J = 0, K = 1 |
| [**D.**](javascript:%20void%200;) | J = 0, K = 0 |

**Answer:** Option **D**

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| 8. Which of the following describes the operation of a positive edge-triggered *D* flip-flop? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | If both inputs are HIGH, the output will toggle. | | [**B.**](javascript:%20void%200;) | The output will follow the input on the leading edge of the clock. | | [**C.**](javascript:%20void%200;) | When both inputs are LOW, an invalid state exists. | | [**D.**](javascript:%20void%200;) | The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock. |   **Answer:** Option **B** |

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| 9. What does the triangle on the clock input of a *J-K* flip-flop mean? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | level enabled | | [**B.**](javascript:%20void%200;) | edge-triggered |   **Answer:** Option **B**   |  |  | | --- | --- | | 10. | A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is \_\_\_\_\_\_\_\_. | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | constantly LOW | | [**B.**](javascript:%20void%200;) | constantly HIGH | | [**C.**](javascript:%20void%200;) | a 20 kHz square wave | | [**D.**](javascript:%20void%200;) | a 10 kHz square wave | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | |  | | --- | | 11. The toggle condition in a master-slave *J-K* flip-flop means that *Q* and https://www.indiabix.com/_files/images/digital-electronics/basic-digital-electronics/mcq10_1019_1.jpg will switch to their \_\_\_\_\_\_\_\_ state(s) at the \_\_\_\_\_\_\_\_. | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | opposite, active clock edge | | [**B.**](javascript:%20void%200;) | inverted, positive clock edge | | [**C.**](javascript:%20void%200;) | quiescent, negative clock edge | | [**D.**](javascript:%20void%200;) | reset, synchronous clock edge |   **Answer:** Option **A**   |  | | --- | | 12. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when \_\_\_\_\_\_\_\_. | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | the clock pulse is LOW | | [**B.**](javascript:%20void%200;) | the clock pulse is HIGH | | [**C.**](javascript:%20void%200;) | the clock pulse transitions from LOW to HIGH | | [**D.**](javascript:%20void%200;) | the clock pulse transitions from HIGH to LOW |   **Answer:** Option **C**   |  | | --- | | 13. What is the hold condition of a flip-flop? | | |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | both *S* and *R* inputs activated | | [**B.**](javascript:%20void%200;) | no active *S* or *R* input | | [**C.**](javascript:%20void%200;) | only *S* is active | | [**D.**](javascript:%20void%200;) | only *R* is active |   **Answer:** Option **B** | | | | |  | |
| 14. The symbols on this flip-flop device indicate \_\_\_\_\_\_\_\_.  https://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq7_00300.gif |
| |  |  |  |  | | --- | --- | --- | --- | | **[A].** | |  |  | | --- | --- | | triggering takes place on the negative-going edge of the CLK pulse | @ | | | **[B].** | triggering takes place on the positive-going edge of the CLK pulse | | **[C].** | triggering can take place anytime during the HIGH level of the CLK waveform | | **[D].** | triggering can take place anytime during the LOW level of the CLK waveform |   **Answer:** Option **A** |

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| 15. What is the significance of the *J* and *K* terminals on the J-K flip-flop? |
| |  |  | | --- | --- | | [**A.**](javascript:%20void%200;) | There is no known significance in their designations. | | [**B.**](javascript:%20void%200;) | The *J* represents "jump," which is how the *Q* output reacts whenever the clock goes high and the *J* input is also HIGH. | | [**C.**](javascript:%20void%200;) | The letters were chosen in honor of Jack Kilby, the inventory of the integrated circuit. | | [**D.**](javascript:%20void%200;) | All of the other letters of the alphabet are already in use. |   **Answer:** Option **C** |